UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/636,131	08/06/2003	Mun-Mo Jeong	8750-044	2385

7590 12/30/2004

MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, OR 97205

EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 12/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/636,131	JEONG ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 6-20 in the reply filed on October 12, 2004 is acknowledged. Claims 1-5 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Specification

The disclosure is objected to because of the following informalities: On page 8, the last line, the examiner suggest replacing "methof" with –method--.

Appropriate correction is required.

Claim Objections

Claim 8 is objected to because of the following informalities: applicant claims that "the portion of the first capping material is approximately half the thickness of the first capping material". The examiner believes applicant intended on reciting "the protruded portion of the first capping material is approximately half the thickness of the first capping material".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6, 10, 14, 16, 17, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In re claims 6 and 17, where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "bitline contact" in claims 6 and 17 is used by the claims to mean "bitline contact hole" or "bitline contact opening", while the accepted meaning is "an electrical connection for a bitline." The term is indefinite because the specification does not clearly redefine the term. Furthermore, it is clear that a conductive interconnection such as a bitline contact cannot be made by "etching the insulating layer". The examiner believes that applicant intended on reciting "forming a bitline contact hole and groove-shaped bitline pattern by etching the insulating film"

In re claim 17, where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition

so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "storage node contact" in claim 17 is used by the claim to mean "storage node contact hole" or "storage node contact opening", while the accepted meaning is "an electrical connection for a bitline." The term is indefinite because the specification does not clearly redefine the term. Furthermore, it is clear that a conductive interconnection such as a storage node contact cannot be made by "etching the third insulating layer". The examiner believes that applicant intended on reciting "forming a storage node contact hole that exposes the storage node contact pad by etching the third insulating film"

Claim 10 recites the limitation "depositing the material" in line 1. There is insufficient antecedent basis for this limitation in the claim. It is unclear if the claim is referring to the first capping layer depositing step or the second capping layer depositing step.

In re claim 14, applicant recited the method of "forming the bitline capping layer". Claim 14 depends from claim 13, which, in turn, depends from claim 7. Claim 7 recites a first and second capping layer. It is unclear which capping layer is being referred to in claim 14.

In re claim 16 and 18, applicant recites that "wherein the order in which the bitline pattern and the bitline contact are formed may be reversed". The examiner notes that there is no clear recitation of the order in which they have been formed, and therefore, it

is unclear what order is in reverse. The examiner notes that this limitation allows for any order of formation of the bitline pattern and the bitline contact, and has been examined accordingly.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 6-9 and 11-12, and 16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Park (U.S. Patent Appl. 2003/0235948).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claim 6, Park discloses method of fabricating a semiconductor device comprising:

forming an insulating film (140, 150, 160) on a semiconductor substrate (105);

forming a bitline contact and a groove-shaped bitline pattern by etching the insulating film (see Figure 4B, 6B, and [0041]-[0049]);

forming a bitline (174) on the bitline contact and a portion of the bitline pattern; and

forming a bitline capping layer (176, 192) on the bitline within the bitline pattern and the insulating film that protrudes from the insulating film, wherein a protruded portion of the bitline capping layer is wider than a width of the bitline (see Figure 9B).

In re claim 7, Park discloses the method wherein forming the bitline capping layer comprises:

depositing a first capping material (176) on an entire surface of the substrate;

etching the first capping material to fill within the bitline pattern on the bitline(see [0049]);

etching the insulating film to a predetermined thickness so that a portion of the first capping material protrudes above the insulating film (see Figure 7B and [0051]);

depositing a second capping material on an entire surface of the substrate; and etching the second capping material so that it remains only on a sidewall of the portion of the first capping material(192, see [0047] for discussion of formation of a spacer).

In re claim 8, Park discloses the method wherein etching the insulating film to the predetermined thickness comprises etching the insulating film to the predetermined thickness so that the portion of the first capping material is approximately half the

thickness of the first capping material (see Figure 7B). The examiner notes that at least half of the first capping material is protruding.

In re claim 9, Park discloses the method wherein depositing the first capping material (176) and depositing the second capping material (192) comprises depositing a material having a wet and a dry etching selectivity with respect to the insulating film (see [0050]-[0051] and [0056]). The examiner notes that

In re claim 11, Park discloses the method wherein forming the bitline capping layer comprises:

forming a pillar-type first capping material (176) on the bitline within the bitline pattern that protrudes from the insulating film; and

forming a sidewall spacer type second capping material (192) on a portion of the first capping material that protrudes from the insulating film, and forming the pillar-type first capping material and forming the sidewall spacer type second capping material so that the bitline capping layer has a stud type structure (see Figure 9B).

In re claim 12, Park discloses the method wherein forming the bitline comprises:

depositing a conductive material (172 in Figure 6B and 174 in text) on an entire surface of the substrate to fill the bitline pattern (see [0048]) ; and

over-etching the conductive material using at least one process chosen from the group consisting of a CMP process and a etch back process so that the conductive material fills up a portion of the bitline pattern to form the bitline (see [0048]).

In re claim 16, Park discloses the method wherein forming the bitline contact and the groove- shaped bitline pattern by etching the insulating film comprises using a dual damascene process (see Figure 6B, bitline contact hole formed within 140 and groove-shaped bitline pattern formed in 150, 160) wherein the order in which the bitline pattern and the bitline contact are formed may be reversed.

In re claim 17, Park discloses a method of fabricating a semiconductor device comprising:

forming a first insulating film (130) having a bitline contact pad (135b) and a storage node contact pad (135a) on a semiconductor substrate (105);

forming a second insulating film (140, 150) on an entire surface of the substrate;

forming a groove-shaped bitline pattern and a bitline contact that exposes the bitline contact pad by etching the second insulation film;

forming a bitline (172, 174) in a portion of the bitline pattern that is connected with the bitline contact pad through the bitline contact;

forming a bitline capping layer (176, 192) on the bitline within the bitline pattern and the insulating film that protrudes from the second insulating film, wherein a protruded portion is wider than a width of the bitline pattern (see Figure 9B);

forming a third insulating film(160) on an entire surface of the substrate; and

forming a storage node contact (190) that exposes the storage node contact pad by etching the second and the third insulating films (140, 160, see [0051] and Figure 9A).

In re claim 18, Park discloses the method wherein forming the groove-shaped bitline pattern and the bitline contact comprises using a dual damascene process (see Figure 6B, bitline contact hole formed within 140 and groove-shaped bitline pattern formed in 150, 160), wherein the order in which the bitline pattern and the bitline contact are formed may be reversed, and wherein the bitline contact pad is used as an etching stop film to form the bitline contact.

In re claim 19, Park discloses the method wherein forming the bitline capping layer comprises:

forming a pillar type first capping material (176) on the bitline within the bitline pattern that protrudes from the second insulating film; and

forming a sidewall spacer type second capping material (192) on a protruded portion of the first capping material and on the second insulating film, wherein the protruded portion of the bitline capping layer has a stud type structure.

In re claim 20, Park discloses the method , wherein forming the storage node contact comprises:

etching the second and the third insulating films (140, 160) using the second capping material of the bitline capping layer as an etching stop film so that the storage node contact is self-align etched (see [0051] [0056] and Figure 9A).

Claims 6-12, 17 and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (U.S. Patent No. 6,281,073).

In re claim 6, Lee discloses a method of fabricating a semiconductor device comprising:

forming an insulating film (119) on a semiconductor substrate (100);

forming a bitline contact and a groove-shaped bitline pattern by etching the insulating film (see Figure 2D and column 5, lines 33-40);

forming a bitline (130) on the bitline contact and a portion of the bitline pattern; and

forming a bitline capping layer (132, 133a) on the bitline within the bitline pattern and the insulating film that protrudes from the insulating film, wherein a protruded portion of the bitline capping layer is wider than a width of the bitline.

The examiner notes that the bitline pattern defines the region that the bitline will be formed, therefore anything formed within the region that the bitline is formed is considered within the bitline pattern region or area.

In re claim 7, Lee discloses the method wherein forming the bitline capping layer comprises:

depositing a first capping material (132) on an entire surface of the substrate;

etching the first capping material to fill within the bitline pattern on the bitline see column 5, lines 53-60);

etching the insulating film to a predetermined thickness so that a portion of the first capping material protrudes above the insulating film (see column 5, lines 33-40);

depositing a second capping material (133) on an entire surface of the substrate; and etching the second capping material so that it remains only on a sidewall of the portion of the first capping material (see column 5, lines 55-68).

In re claim 8, Lee discloses the method wherein etching the insulating film to the predetermined thickness comprises etching the insulating film to the predetermined thickness so that the portion of the first capping material is approximately half the thickness of the first capping material. The examiner notes that at least half of the first capping material is exposed.

In re claim 9, Lee discloses the method wherein depositing the first capping material (132 of a nitride in one embodiment) and depositing the second capping material (133 of nitride) comprises depositing a material having a wet and a dry etching selectivity with respect to the insulating film (119 including an oxide, see column 5, line 55 through column 6, line 10).

In re claim 10, Lee discloses the method wherein depositing the material comprises depositing a film (133) from a silicon nitride film series, and forming the insulating film comprises forming a film from an oxide film series (119, see column 25-35).

In re claim 11, Lee discloses the method wherein forming the bitline capping layer comprises:

forming a pillar-type first capping material (132) on the bitline within the bitline pattern that protrudes from the insulating film; and

forming a sidewall spacer type second capping material (133) on a portion of the first capping material that protrudes from the insulating film, and forming the pillar-type first capping material and forming the sidewall spacer type second capping material so that the bitline capping layer has a stud type structure.

In re claim 12, Lee discloses the method wherein forming the bitline comprises:

depositing a conductive material (130) on an entire surface of the substrate to fill the bitline pattern; and

over-etching the conductive material using at least one process chosen from the group consisting of a CMP process and a etch back process so that the conductive material fills up a portion of the bitline pattern to form the bitline (see column 5, lines 55-60). The examiner reads the masking and etching of the bitline to be etching back since some of the bitline conductive material is "etched back" to the insulating layer and removed.

In re claim 17, Lee discloses a method of fabricating a semiconductor device comprising:

forming a first insulating film (113) having a bitline contact pad (120b) and a storage node contact pad (120a) on a semiconductor substrate;

forming a second insulating film (119) on an entire surface of the substrate;

forming a groove-shaped bitline pattern and a bitline contact that exposes the bitline contact pad by etching the second insulation film (see column 5, lines 33-40);

forming a bitline (130) in a portion of the bitline pattern that is connected with the bitline contact pad through the bitline contact;

forming a bitline capping layer (132, 133) on the bitline within the bitline pattern and the insulating film that protrudes from the second insulating film, wherein a protruded portion is wider than a width of the bitline pattern;

forming a third insulating film (135) on an entire surface of the substrate; and

forming a storage node contact (see Figure 2g) that exposes the storage node contact pad by etching the second (119) and the third insulating (135) films (see column 6, lines 10-40).

In re claim 19, Lee discloses the method wherein forming the bitline capping layer comprises:

forming a pillar type first capping material (132) on the bitline within the bitline pattern that protrudes from the second insulating film; and

forming a sidewall spacer type second capping material (133) on a protruded portion of the first capping material and on the second insulating film, wherein the protruded portion of the bitline capping layer has a stud type structure.

In re claim 20, Lee discloses the method wherein forming the storage node contact comprises:

etching the second and the third insulating films using the second capping material of the bitline capping layer as an etching stop film so that the storage node contact is self-align etched (see column 6, lines 10-40).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-15 are rejected under 35 U.S.C. 103(a) as being obvious over Park et al. (U.S. Patent Appl. 2003/0235948) in view of Lee et al. (U.S. Patent Appl. 2002/0115256).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the

reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

In re claim 13, Park discloses the method as claimed and rejected above including the method of forming the insulating layer of an upper oxide film, a lower oxide film and forming an etching stop layer between the upper and lower oxide film (see [0042]). Park does not disclose the method wherein the etching stop layer is a silicon nitride. Lee et al. disclose the method of utilizing a silicon nitride layer as an etching stop layer in an ILD stack of silicon oxide, silicon nitride, and a silicon oxide 110, 116, and 118, see [0039], [0042], [0047]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a silicon nitride as a etching stop layer for an ILD stack, because as silicon nitride has a good etching selectivity with respect to silicon oxide and because the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945) See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960) (selection of a known plastic to make a container of a type made of plastics prior to the invention was held to be obvious); Ryco, Inc. v. Ag-Bag Corp., 857 F.2d 1418, 8 USPQ2d 1323 (Fed. Cir. 1988).

In re claim 14, the combined Park and Lee et al. disclose the method wherein forming the bitline capping layer comprises: etching the upper oxide film using the silicon nitride film as an etching stop film (see Park [0042]-[0049]).

In re claim 15, the combined Park and Lee et al. disclose the method wherein etching the second capping material comprises: etching the lower oxide film so that it remains under the second capping material (see Park [0056]).

Claims 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent No. 6,281,073, referred to as Lee) in view of Lee et al. (U.S. Patent Appl. 2002/0115256, referred to as Lee et al.).

Lee discloses the method as claimed and rejected including the method of forming an interlayer dielectric layer of a mixture silicon oxide and silicon nitride, but does not specifically state the method of forming the insulating layer comprises: forming an upper oxide film; forming a lower oxide film; and forming a silicon nitride film between the upper and the lower oxide films.

Lee et al. discloses the method of forming a silicon oxide, silicon nitride, silicon oxide interlayer dielectric film including forming an upper oxide film; forming a lower oxide film; and forming a silicon nitride film between the upper and the lower oxide films (110, 116, 118, see [0039], [0042], [0047]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form an interlayer dielectric including an ONO film because as Lee teaches a combination of silicon oxide and silicon nitride may be used and because as Lee et al. teaches, the combination of an ONO film allows for etching selectivity and since it has been held that the selection of a known material based on its suitability for its intended use supported a prima facie

obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945) See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960) (selection of a known plastic to make a container of a type made of plastics prior to the invention was held to be obvious); Ryco, Inc. v. Ag-Bag Corp., 857 F.2d 1418, 8 USPQ2d 1323 (Fed. Cir. 1988).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk